

HELENA : A NEW SOFTWARE FOR THE DESIGN OF MMICS

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Abstract: *HELENA*, a new software for device optimization and circuit design is presented. This software provides for any kind of HEMT the DC, AC and noise properties in the cm and mm wave range. It is very fast, easy to use and needs only personal computer.

I-INTRODUCTION

For the design of MMICs, and more generally for the optimization of circuits using HEMTs, the knowledge of the high frequency parameters including the noise parameters constitutes a key point. Since measurements on test device are difficult (especially for the noise parameters), a theoretical modeling is very well suited if it is in good agreement with experiments. For this purpose a new HEMT software called HELENA for Hemt ELEctrical properties and Noise Analysis has been developed. The main features of this modeling are the following:

- very easy to use even for people not familiar with device modeling.
- very fast, needs only personal computer.
- all kinds of HEMTs, including conventional HEMT, pseudomorphic on GaAs, lattice matched on InP, can be studied.
- the device properties, small signal equivalent circuit and noise, are given in a very large frequency range including the millimeter wave range.
- the theoretical results are in a very good agreement with experimental results.

The flow chart of HELENA is given in figure 1

It is divided in three blocks :

- The layer analysis
- The device performance modeling
- The results display

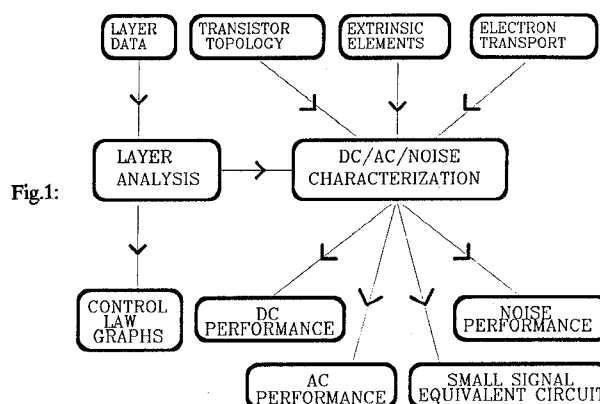


Fig.1:

II-THE LAYER ANALYSIS

The purpose of this routine is to obtain the charge control law by a schottky barrier of any HEMT active layer. The input parameters (see fig. 2-a) are the thickness, doping (bulk or planar) and composition (%In, %Al) of each layer constituting the active layer.

LAYERS DATA INPUT				
Type 1	T= 300 K	Edx= 0.023 eV		
Layers	Thickness (Å)	Doping (At/cm ³)	% In	% Al
GaAs	599.00	2.0000E+24	0.000	0.000
	125.00	1.0000E+20	0.000	0.200
AlInAs	50.00	0.0000E+24	0.000	0.200
	20.00	1.0000E+20	0.000	0.200
GaInAs	120.00	1.0000E+20	0.150	0.000
	0.00	1.0000E+20	0.000	0.200
AlInAs	0.00	2.0000E+24	0.000	0.200
	0.00	1.0000E+20	0.000	0.200
GaAs	1000.00	1.0000E+20	0.000	0.000

fig. 2-a: Layer structure

This modeling is based on a simplified selfconsistent resolution of Schrodinger and Poisson's equations. As the matter of fact, J. ALAMKAN (1) has shown that the two first energy subbands are related to the sheet carrier density in 2DEG by the relation

$$E_i = A_i + B_i \cdot N_S \quad [1]$$

where A_i and B_i are two constants and N_S is the sheet carrier density.

This result allows us to write a simplified charge control law for electrons in the 2DEG as [2]. This relation can be considered as an implicit $E_F(N_S)$ relationship.

$$N_S = \frac{D \cdot k \cdot T}{q} \sum_i \ln \left(1 + \exp \frac{E_F - E_i}{k \cdot T} \right) \quad [2]$$

In this expression, D is the density of states, k the Boltzmann constant, E_F the Fermi level, q the electron charge and T the temperature. The electron supplying layer for which quantum effects are negligible is classically described using Fermi statistic. Layer analysis provides for each layer the sheet carrier density (ionized donor and free carrier density), and associated capacitances as a function of the gate voltage. Figure 2-b shows the charge control law in terms of capacitances in the 2DEG and in the electron supplying layer for the layer shown fig. 2-a.

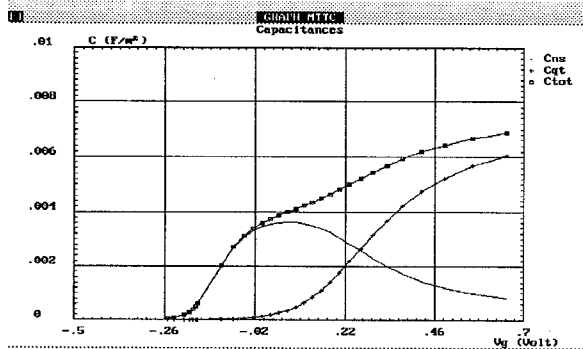


fig 2-b: Charge control law

A good agreement between this modeling and measurements has been obtained. Any HEMT structure like conventional HEMT (GaAlAs / GaAs), lattice matched on InP (GaInAs / InP) can be investigated in the same way. The main advantage of this approximation is to be very fast as compared with selfconsistent approach and to be sufficiently accurate.

III-THE DEVICE MODELING

The device modeling is performed using a quasi 2D approach (2),(3). In this approach the charge control law (in terms of sheet carrier density) is associated with an electron transport law to give the DC, AC and Noise properties. The input parameters of this routine are the transistor topology (see Fig. 3-a), the charge control law given by the layer analysis previously described, the electron transport law and the extrinsic parameters of the small signal equivalent circuit. For the electron transport law, both simple $v(E)$ relationship (suitable for fitting experimental data) or hydrodynamic equation (suitable for device performances predictions) can be used. A realistic structure including gate recess

(fig. 3-a) as well as surface potential and carrier injection into the buffer is taken into account.

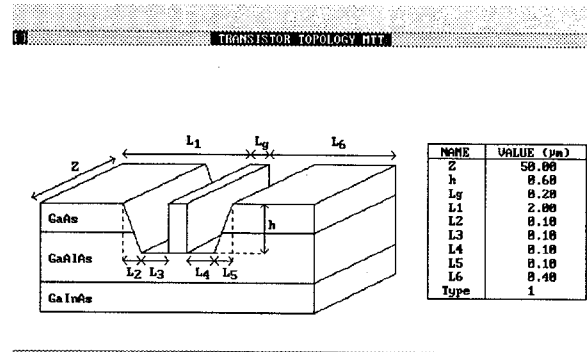


fig. 3-a: Device structure

III-a : DC AND AC CHARACTERISTICS

In this step, only intrinsic parameters are studied. As boundary condition, the electric field is imposed at the source end of the channel. For given V_{gs} and I_{ds} , electron transport and Poisson's equation are combined to give a quadratic equation (4). Solving this equation at each step from source to drain gives the quantities of physical interest in the channel: Electric field, electron velocity, electron energy... Drain to source voltage is obtained by integrating the electric field from source to drain. The DC characteristics $I_{ds}(V_{gs}, V_{ds})$ are then computed (see Fig. 3-b).

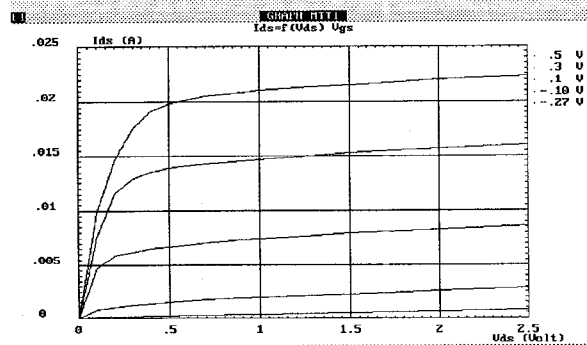


fig 3-b: DC characteristics

At each DC point, the AC performance (S-parameters or small signal equivalent circuit) is computed using the active line approach (5). In this method, a local small signal equivalent circuit is defined for each slice $(x, x + dx)$. Electrical properties in terms of admittance are calculated step by step from source to drain following the method described in (5), and the small signal equivalent circuit for the whole device is then deduced. This small signal equivalent circuit depends not only on biasing condition, but also on frequency. A feature of this approach is to provide not only the main small signal parameters (G_m , G_d , C_{gs} , C_{gd}) but also R_i , R_{gd} ,

τ , C_{ds} which are very important for the determination of high frequency device behaviour (see Fig.3-c).

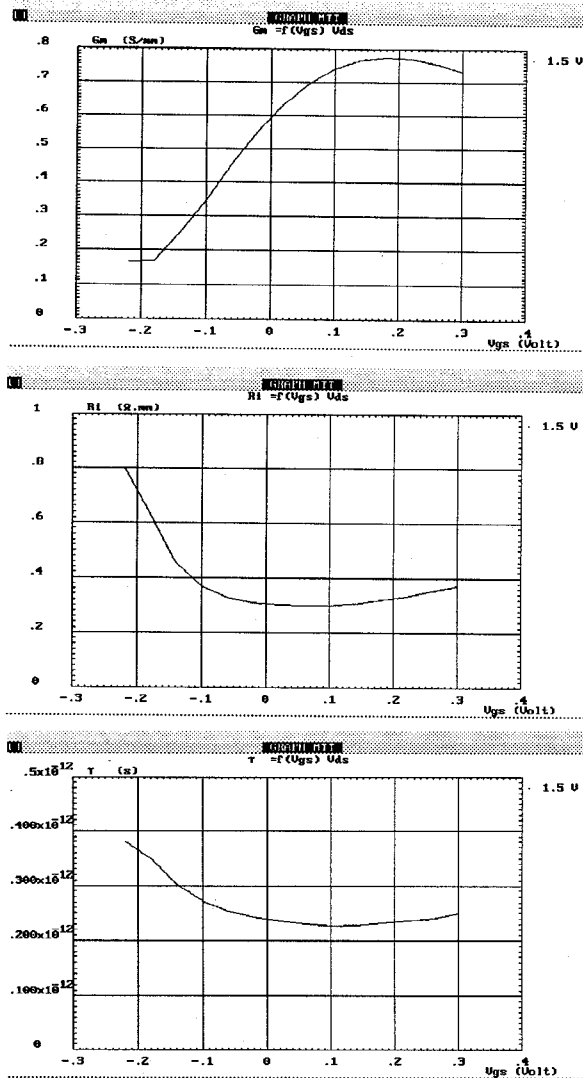


Fig. 3-c: AC parameters

For a given bias voltage (V_{gs} , V_{ds}), all these parameters are summarized in a schematic small signal equivalent circuit (see fig.3-d).

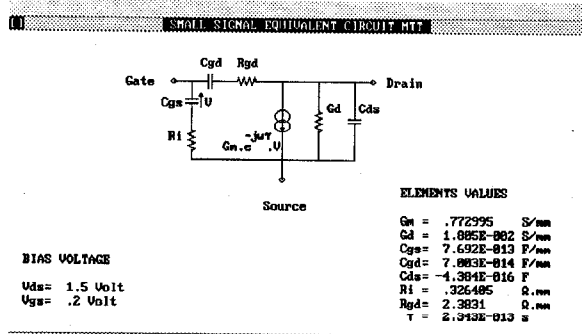


Fig. 3-d: Small signal equivalent circuit

III-b: NOISE MODELING

For each DC point, the four noise parameters F_{min} , R_n , G_n , Γ_{opt} as well as associated gain (G_{ass}) and maximum available gain (MAG) are computed. These calculations are performed in two steps: the intrinsic device is first considered and after that the extrinsic elements (inductance, capacitance, resistance) are introduced (see fig 3-e). The intrinsic noise modeling is achieved using the well-known impedance field method. This impedance field is deduced from the active line as described in (5). The main advantage of this method is its validity in the mm wave range as compared with the conventional approach based on quasi static modeling. This modeling provides the noise correlation matrix of the noisy intrinsic transistor. At this step, the intrinsic device is described by two matrices (admittance and correlation) and any device propertie can be deduced from these matrices.

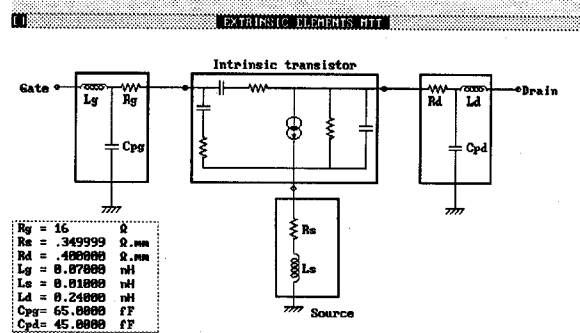
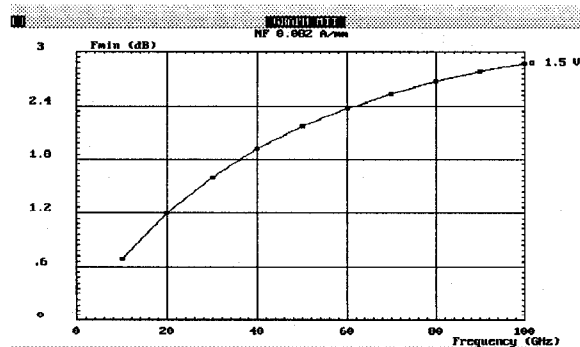


fig. 3-e: Extrinsic elements

The second step is the calculation of the noise performance for the extrinsic device. This is performed by simple matrix manipulation using the method described in (6). When the noise characterization is completed, the graphs of the HEMT noise parameters can be view versus drain current or frequency in order to specify the optimum DC bias condition and the frequency dependence of device performance. These graphs (see fig 3-f) are given in a convenient form (ex: dB scales for F_{min} or Smith chart for Γ_{opt}).



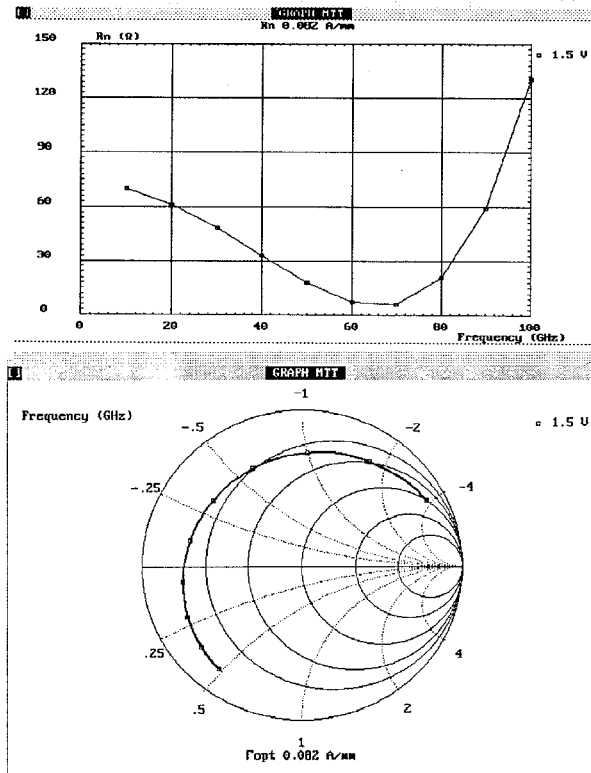


fig 3-f:

It should be noted that all the figures of this paper (except fig.1) are screens of HELENA software. HELENA software has been written in CAD-aimed way. All the physical and technological data are easily introduced and file-managed thanks to pull-downs menus, data illustrations and mouse uses. It's as easy to use HELENA as a Macintosh software. The user has just to click the mouse's button to run a data acquisition, a characterization or view the characterization output.

IV-COMPARISON WITH EXPERIMENTS

Figure 4 shows comparison between theory and measurements made on a device having the active layer and topology shown in figures 2-a and 3-a. This figure shows a good agreement between theory and experimental findings.

V-CONCLUSION

We have developed a new HEMT modeling well suited for device performance analysis and circuit optimization. This quasi-2D modeling takes into account many physical phenomena that occur in a submicrometer gate FET's. A complete analysis of device is carried out and results are in a good agreement with measurements. This analysis is included in a convenient software

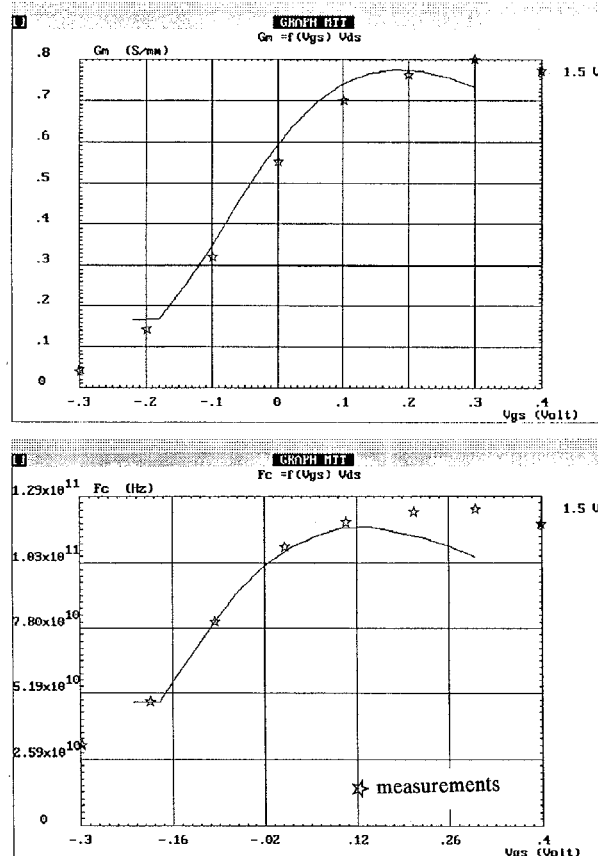


fig. 4

very easy to use, very fast, with advantage to display result in a convenient form. For each DC point, few seconds only on Personal Computer are needed to obtained the AC and noise performances. This software will be available in the near future.

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